**Step 1:- First Create 2:1 Mux :-**

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-- Company:

-- Engineer:

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-- Create Date: 12:24:59 09/25/2017

-- Design Name:

-- Module Name: MUX2TO1 - Behavioral

-- Project Name:

-- Target Devices:

-- Tool versions:

-- Description:

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-- Dependencies:

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-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

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library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_ARITH.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

---- Uncomment the following library declaration if instantiating

---- any Xilinx primitives in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity MUX2TO1 is

Port ( A : in STD\_LOGIC;

B : in STD\_LOGIC;

S : in STD\_LOGIC;

E : in STD\_LOGIC;

Y : out STD\_LOGIC);

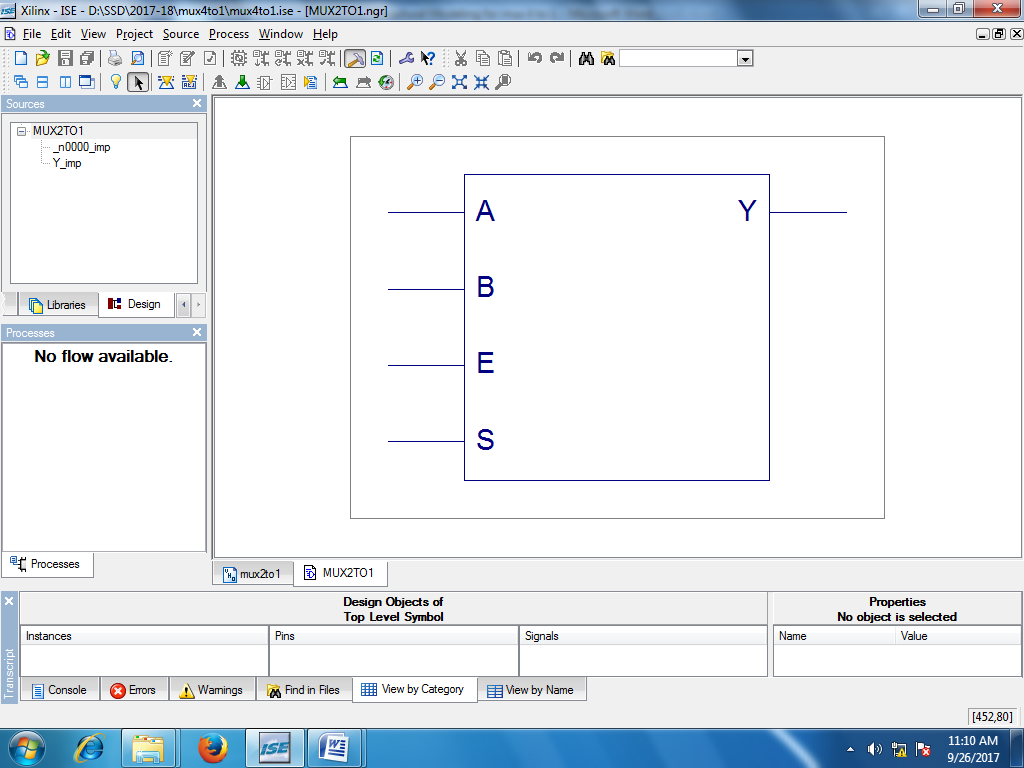
end MUX2TO1;

architecture Behavioral of MUX2TO1 is

begin

Y<= NOT E and ( (( NOT S AND A) OR (B AND S) ));

end Behavioral;



**Step 2:- Create 4:1 using 3 2:1 Muxes**

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-- Company:

-- Engineer:

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-- Create Date: 10:57:47 09/26/2017

-- Design Name:

-- Module Name: m4to1 - Behavioral

-- Project Name:

-- Target Devices:

-- Tool versions:

-- Description:

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-- Dependencies:

--

-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

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library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_ARITH.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

---- Uncomment the following library declaration if instantiating

---- any Xilinx primitives in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity m4to1 is

Port ( a : in STD\_LOGIC;

b : in STD\_LOGIC;

c : in STD\_LOGIC;

d : in STD\_LOGIC;

s0 : in STD\_LOGIC;

s1 : in STD\_LOGIC;

E: in STD\_LOGIC;

y : out STD\_LOGIC);

end m4to1;

architecture Behavioral of m4to1 is

component MUX2TO1 is

Port ( A : in STD\_LOGIC;

B : in STD\_LOGIC;

S : in STD\_LOGIC;

E: in STD\_LOGIC;

Y : out STD\_LOGIC);

end component;

signal y1,y2: std\_logic;

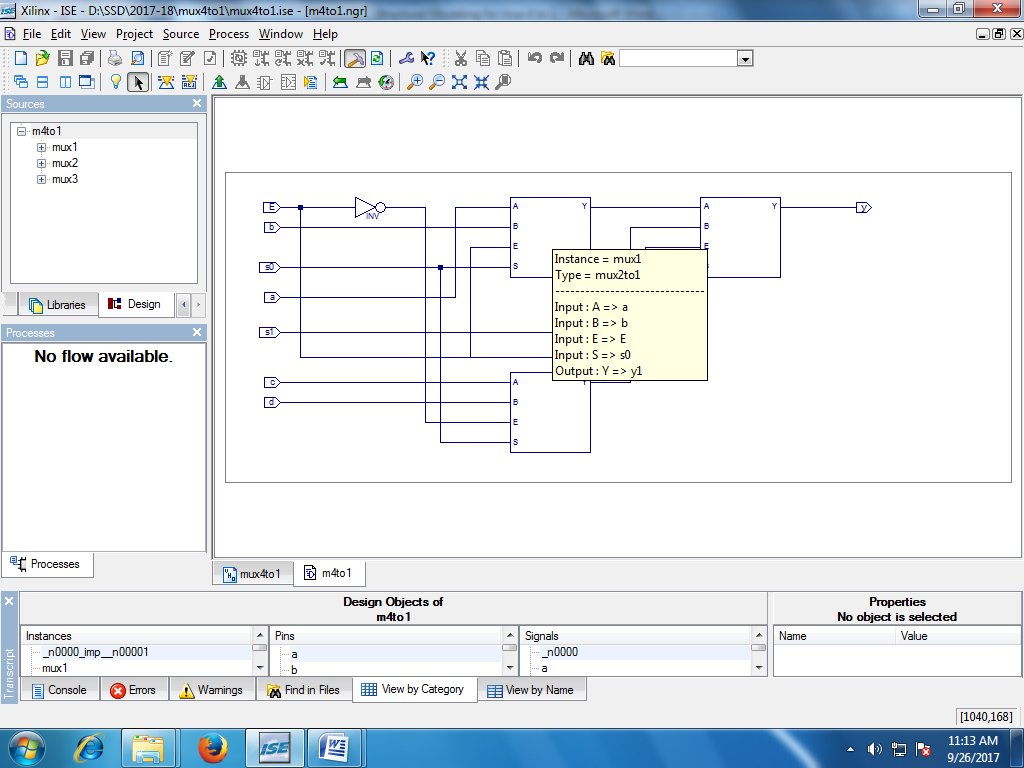
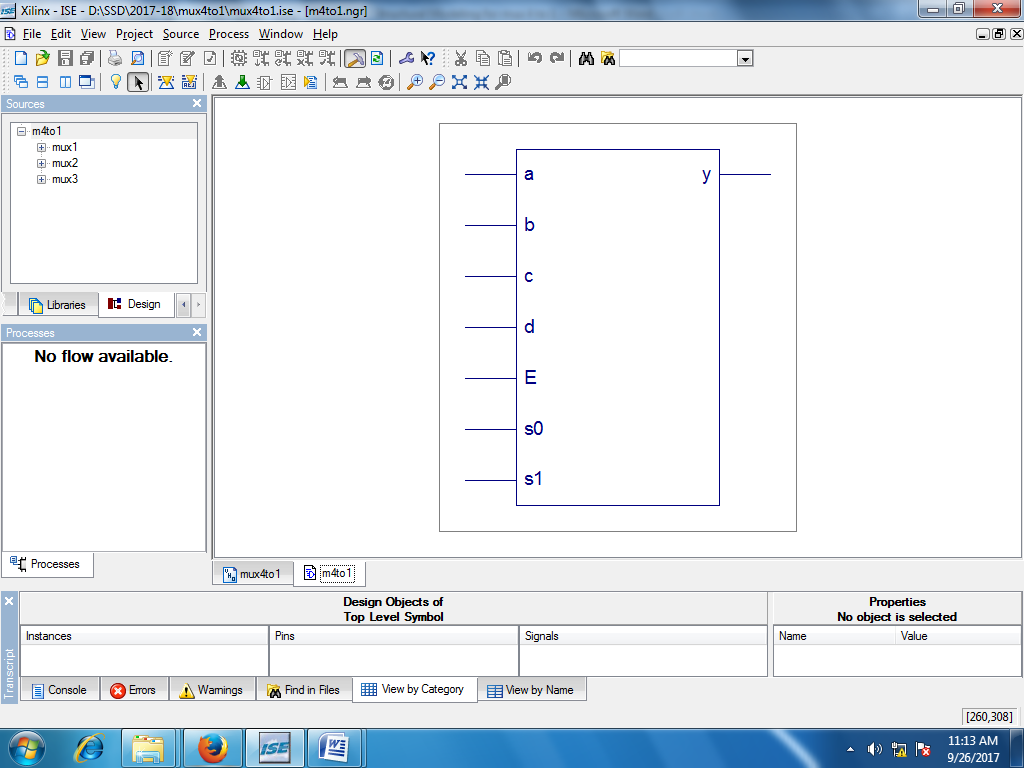
begin

mux1 : mux2to1 port map (a,b,s0,E,y1);

mux2 : mux2to1 port map (c,d, s0,not E,y2);

mux3 : mux2to1 port map (y1,y2,s1,E,y);

end Behavioral;

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Output:-

